A Novel Method of Realisation of Dispersed Optimal Beam Steering Architecture for Active Phased Array Radar

D.Govind Rao[1],Anant Raut[2], Renuka Prasad[3],Md Mustakim[4],K Sreenivasulu[5]
Electronics and Radar Development Establishment, DRDO, Bangalore
dgrao@lrde.drdo.in

Abstract:

This paper depicts architecture of the phased array Radar where few thousands of radiating elements are controlled through the FPGA based hardware. The phased array consists of several thousand of Transmit and Receive Modules. These modules are controlled through an algorithm developed by us. The FPGA based hardware is developed in an hierarchical method to distribute the functions so that the functional, timing and interface requirement are met. In this approach Spartan FPGA's are used for the computation and timing generation. The dispersed beam steering architecture designed and developed to steer the beam in the desired direction using the phase scanning method. In Phase Scanning, the beam of an antenna points in a direction that is normal to the phase front. In phased arrays, this phase front is adjusted to steer the beam by individual control of the phase of excitation of each radiating element. The distributed architecture developed is using the optimal resources of the FPGA and it Reconfigurable in nature.

Key Words: ***TRM, Spartan FPGA, Calibration, MATLAB, Beam Steering, Phase, Attenuation, DBF, MSTC.***

I INTRODUCTION

The modern day Active Phased Radar is a very complex system; consist of thousands of radiating antenna elements, dedicated transmitters and receivers for each antenna element. Group level transmitters and receivers for the cluster of sub arrays spread across the antenna elements. All these subsystems are connected to each other through dedicated digital communication link. The RF energy is also distributed in the same limited spaced antenna frame. The flow of beam steering logic has to pass through this hierarchical arrangement of subsystems keeping in mind the optimum and accurate addressing for each antenna element. The beam steering architecture presented here is designed in such a manner that fine control over each and every antenna element is established without causing additional distribution delay.

The computation of phase commands for the phase shifters which are present inside the transmit/receive modules are done at the group level controllers which are implemented inside the FPGAs with optimum timing and resource utilization. This yielded a distributed beam steering architecture with smallest possible beam switching time. As the beam switching time is a very important parameter of active phased array radar, development of this architecture is a major mile stone in the development of active phase radar.

II DESIGN METHODOLOGY

The state of the art technology radars are very complex and hardware intensive. It is required to develop architecture to control several thousands of radiating elements. As mentioned in the antenna theory, several thousand antenna array is required to construct a pencil beam. After constructing the antenna it is required to develop a methodology to control each one of the element for loading the phase and attenuation value.

The architecture developed is implemented in large number of Beam steering controllers as shown in figure 1. There are N numbers of beam steering controllers in the phased array to steer the beam from one direction to otherdirection. The synchronization of all of them together; in order to get precise accuracy in outputs in terms of phase values and timing, was a challenging task. The architecture designed utilizes the concurrent computation capabilities of FPGAs. High speed optical communication links are used to achieve faster data transfer. The design has taken in a modular approach, in which different modules in the FPGA are reused in time sharing basis, in order to optimize the resources. The verification of the algorithm is done using the state of the art verification tools available for FPGA verification.

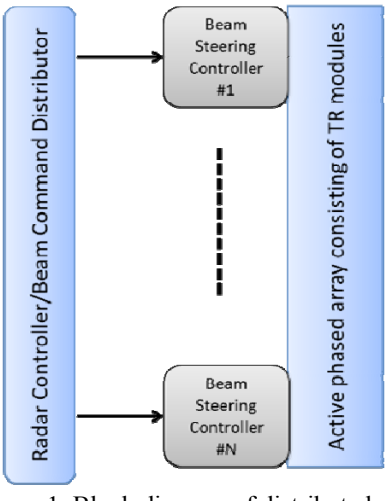

Figure 1. Block diagram of distributed architecture

IIIFPGA BASED ARCHITECTURE DEVELOPMENT

To meet the requirement of large number of beam steering controllers in the phased arraythe architecture is divided into N number of Beam steering controller. In each one of the beam steering controller the sparatn FPGA has been chosen for the computation of phase values and timing generation.

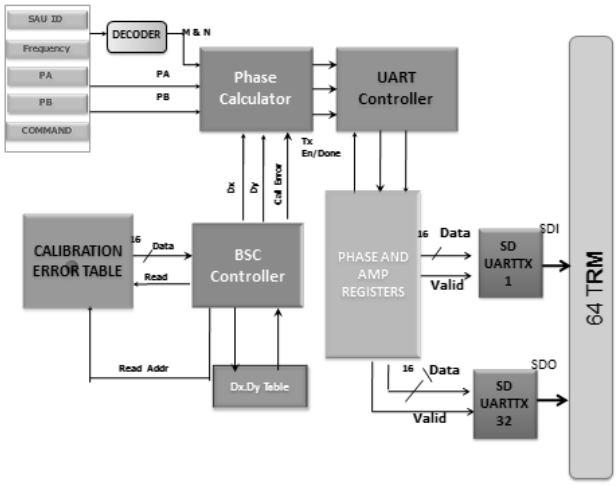

Figure 2: FPGA based Beam steering controller architecture

The algorithm developed is working successfully in the radar without any glitches or errors. Using this algorithm; the radar is able to scan the desired volume of interest accurately and swiftly. This is a novel method adopted for the development of Dispersed beam steering architecture using multiple FPGA's. The method developed is modular in nature and generic architecture can be adapted to any kind of active Phased Array Radar Systems.

Design challenges faced to implement this architecture are:

- Triangular grid Structure of antenna array.
- Locating dx and dy accurately (element spacing)
- Finding co-ordinate of each element.
- Sub array position mapping from sub array ID

The figure2 shows the triangular array grid for one sub array.

The Sub Array Unit is responsible for controlling 64 TR elements in both Transmit and Receive Modes. 64 Elements are arranged in a matrix form as shown in the Figure 1

A simple and efficient way of implementing the distributed active array architecture is designed and realized in this paper. It consists of Radar Computer (RC), Synchronization Unit, tens of Sub Array Unit (SAU) and hundreds of Transmit

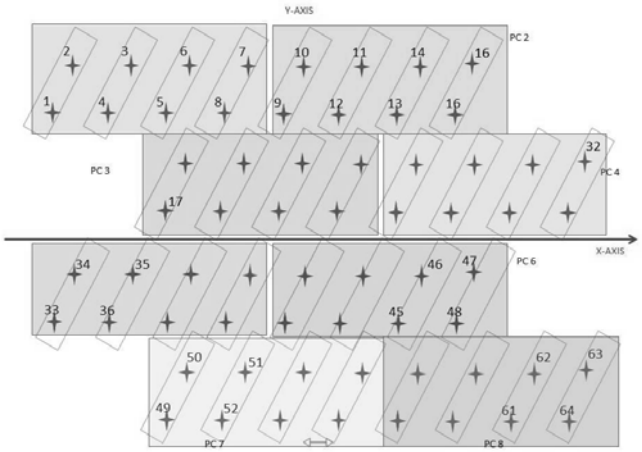

Figure 2: Antenna Element Grid Array

and Receive Modules (TRM) as shown in the Figure 2.

There are 24 SAUs and each SAU controls and commands 64 TR elements. This architecture is designed to have programmability at each level in the hierarchy every unit is based on Field Programmable Devices (FPGA)[2]. FPGA's of great significance which provides much flexibility for the designers like massive parallel processing, quick system design, higher performance and lower design costs etc. The beam steering network is designed in two levels of hierarchy; 1) Sub Array Unit (SAU) and 2).Transmit and Receive Modules (TRM).

In each level of hierarchy FPGA's have been used to provide flexibility and grater re-programmability to function in all the different modes of operation. Each one of the FPGA's control Logic is designed and developed to meet the timing requirements and interface requirements for beam steering. The Optical Aurora link and serial communication UART protocol has been implemented for communicating the data.

The beam scheduler plans ahead the future beam position and accordingly commands the Radar Computer. The Radar computer sends this data to synchronization unit and further synchronization unit broadcasts these messages to Sub Array Units. On receipt of the beam parameters, sub array unit will compute required phase and amplitude for all the 64 elements and communicates the phases to each TR controller unit which configures the TR element with new phase.

Acknowledgement for each message communicated between systems is also defined for reliable communication and integration.

The Sub Array Unit (SAU) interfaces with Synchronization Unit one side and Transmit Receive Module (TRMs) on the Array panel. SAU is having FPGA based card which is responsible for receiving the data from the Sync Unitoptical aurora at 3.6 GBPS data rate [9]. The SAU operates different modes like Dwell mode, Calibration mode and status modes. SAU computes phase required for all the 64 elements for steering the beam in Dwell mode of operation.SAU communicates the phase and amplitude to all the 64 TR

elements over similar serial communication at 5 Mbps and controls all the TR elements in the phased array.

The main functions of SAU are to communicate with Sync Unit for command and control, to configurationSAU ID,tocalculatePhase and Amplitude for all the TRMs thenStores Calibration Values in FLASH and Control and Status monitoring of all the TR elements.

The array operated in S- Band and considering transmit frequency as 3.3 GHz, the elemental spacing in both X- Axis and Y- Axis as 45 mm and 54mm respectively.

The Radar Computer calculates the phase gradients required for steering the beam using Azimuth, Elevation, Pitch, Tilt, Roll and Frequency information from Beam scheduler. The Phase gradient is calculated for a 2D Array using following equation:

$$PA = (2\pi / \lambda) * dx * Sin\theta * Cos\Phi \quad \text{.....(i)}$$

$$PB = (2\pi / \lambda) * dy * Sin\theta * Sin\Phi \quad \text{.....(ii)}$$

Where

θ = Azimuth angle in degrees

Φ = Elevation angle in degrees

λ = Operating wavelength in *mt*

dx= Element Spacing in X- axis in *mt*

dy= Element Spacing in Y- axis in *mt*

PA & PB are Phase gradients in azimuth and elevation respectively. θ and Φ vary from -90º to +90º. Considering angular accuracy of 0.1º for both θ and Φ. The phase gradients PA & PB are computed using (i) & (ii). PA & PB values lie in the range of ±3600. Taking one decimal fraction, the decimal value of PA & PB ranges from -36000 to +36000 and represented in 18 bit binary including sign bit. Since optical aurora protocol is based on 16 bit format, 18 bit value is divided by factor of 4 to obtain 16 bit PA & PB and this factor of 4 is compensated later in the calculation of the phase. Better accuracy is maintained during the final phase calculated.

Synchronization Unit will broadcast the beam parameters as received from Radar computer to all Sub Array Units. All the 30 Sub Array Units are configured with a unique ID which defines the row and column position (M, N) of the sub array in the array. Sub Array Unit receives the phase gradients and calculates the phase required for all the 64 elements using the following equation:

$$Phase = ((m*PA + n*PB) \% 3600) / 5.625 * 10 * 4) \pm cal\ Error \quad \text{.....(iii)}$$

Where,

m = dx + 32*N, absolute position of the TR element on the Array wrt X-axis.

dx = relative position of the TR element wrt each Sub Array Unit (SAU) on the X-axis. (8 X 4 = 32, shift of 8 elements are multiplied and added to dx. 64 elements are arranges in 8x8 matrix. Factor 4 is compensated in quantization)

n = dy + 32*M, absolute position of the TR element on the Array wrt Y-axis. (8 X 4 = 32, shift of 8 elements are multiplied and added to dx. 64 elements are arranges in 8x8 matrix. Factor 4 is compensated in quantization)

dy = relative position of the TR element wrt each Sub Array Unit (SAU) on the Y-axis.

M = X co-ordinate of the SAU on the Array.

N = Y co-ordinate of the SAU on the Array.

calerror = Calibration error value of the TR element are stored in the Flash Memory.

The calibration error values are stored in flash and accessed based on the frequency and compensated to obtain final phase TR Element. Both Phase and Amplitude are packetized and sent to TR controller which in turn controls the TR element.

The Beam Steering architecture is designed using Xilinx FPGA residing in the Sub Array Unit. The control Logic of Beam Steering architecture is as shown in Figure 3.

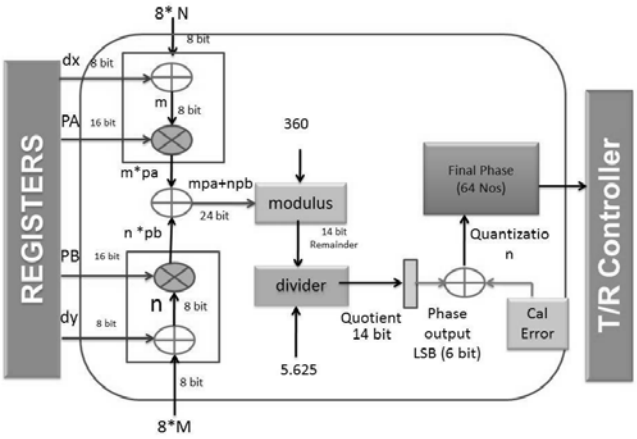

Figure 3: FPGA Control Logic architecture of beam steering

The beam steering logic is designed using logic core blocks. Few important modules of the FPGA control Logic of sub array Unit are described below

- **Multiplier**

Multiplier module is used to realize m * PA and n * PB. This block multiplies 8 bit 'm' or 'n' and 16 bit PA or PB data yielding 24 bit resultant including sign bit. Two such blocks are implemented in parallel to achieve fast computation.

- **Divider and Modulus**

The 24 bit resultant is subjected for modulus operation using 3600 as divisor. This is to bring the phase within 360º (Factor of 10 is considered here since PA and PB are multiplied by 10 at the input). A 14 bit result has to be

quantized for 6 bit phase shifter as shown below:

$$\text{Quantization factor} = 360 / 2^6 = 5.625$$

$$5.625 = \frac{1}{5.625} X \frac{4}{4} X \frac{10}{10}$$

The 14 bit resultant is divided using 5.625 or 225 i.e., 5.625x4x10 = 225. The factor 4 in numerator is compensated in calculation of m & n. The factor 10in the numerator is compensated in PA and PB at the input.

The 14 bit quotient obtained gives the phase given to the phase shifter for steering the beam. LSB [5:0] is sliced from this 14 bit result and fed to an adder for adding Calibration error values.. Calibration table w.r.t frequency is stored in Sub Array Unit and the 6 bit calculated phase is added with the calibration error value. Final phase and amplitude for a particular TR element is thus loaded to obtain beam steering.
All these modulesare designed using parallel multipliers, adders and division blocks and efficiently implemented to reduce the calculation time.

III RESULTS

The Figure 4shows the timing diagram of the phase calculation. 16 bit PA and PB are given as inputs, dx and dy change for different elements and final phase for 64 TR elements are calculated. The final phase and amplitude are calculated sequentially for all the 64 elements after adding calibration values.

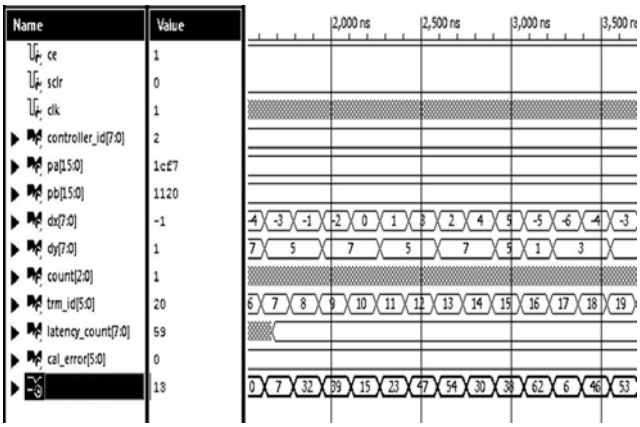

Figure4: Simulation results of beam steering values.

The Beam steering logic is implemented in Spartan 3 Xilinx FPGA. The Figure 5 shows the chipscope signals captured during the calculation of phase values.

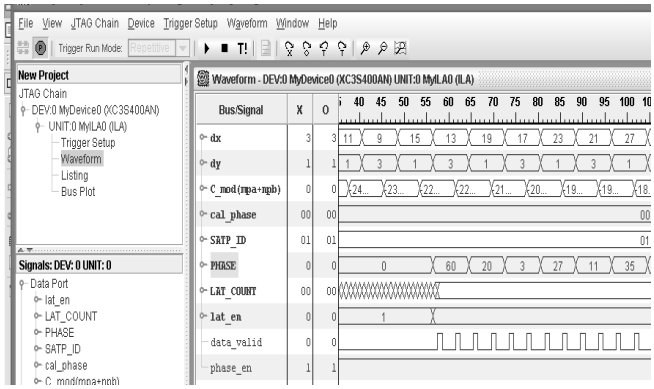

Figure5: Implementation results of beam steering values.

Considering 50 MHz clock input, the phase of the first TR element is calculated after 1.2 usec. 64 elements phase and amplitude values in both Tx and Rx takes additional 63x 8 clock (8 clocks are required between TR element). Total time taken for the calculation of Phase and amplitude is **11.3 usec**. The Sub Array Unit is integrated with 64 elements and such 24 SAUs are integrated in the array and tested in Near Felid Test Range to ascertain the results as shown in figure 6.

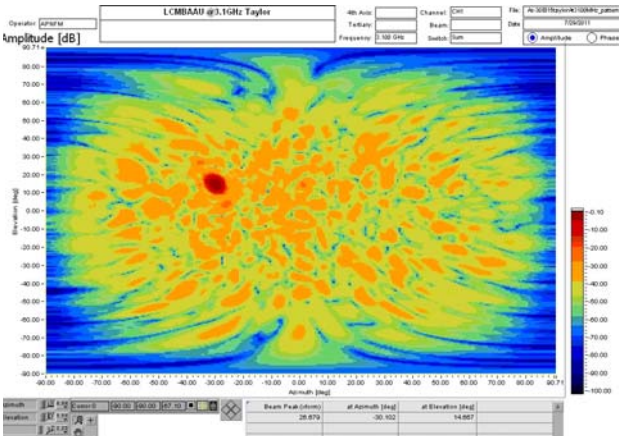

Figure 6 NFTR Result

IVCONCLUSION AND FUTURE SCOPE

The idea presented here depicts the efficient, optimized and distributed beam steering algorithm implemented using state of the art FPGA devices. The architecture is modular and scalable which can be used in different radar system with minimal changes. The algorithm is validated in a near field test range. The algorithm can be further adapted for ASIC implementation for future applications.

The algorithm developed is working successfully in the radar without any glitches or errors. Using this algorithm; the radar is able to scan the desired volume of interest accurately and swiftly. This is a novel method adopted for the development of Dispersed beam steering architecture using

multiple FPGA's. The method developed is modular in nature and generic architecture can be adapted to any kind of active Phased Array Radar Systems.

IXACKNOWLEDGEMENT

We are grateful to Mr. S. Ravind, Director LRDE, Mr. L.G.M Prakasam, Project Director ARUDRHA, LRDE Bangalore for providing this opportunity for development of the Active Phased Array Radar. We are also thankful to Mr. Upendra Shankar Pandey, Scientist, and Mr. Sreenivasulu K, Scientist, LRDE Bangalore for their valuable suggestions and inputs during the development of the system

REFERENCES

[1] Merrill L Skolnik : RADAR HANDBOOK ,TATA McGRAW-HILL, 3nd edition, 2008.
[2] RC.Cofer and Ben Harding"Rapid System Prototyping with FPGAs" Newnes Publishers, 2006.
[3] Merrill L Skolnik : Introduction to Radar Systems,TATAMcGRAW-HILL, 2nd edition, pgs-1,2,5,278-280,322-324,1985.
[4] Bassem R. Mahafza, Ph.D. Radar SystemsAnalysis and Design MATLAB, CHAPMAN & HALL/CRC,2000.
[5] Constantine A. Balanis, "Antenna Theory Analysis and Design", A john wiley& sons, inc., publication, Third Edition, 2005.
[6] Robert J. Mailloux," Phased Array Antenna Handbook", Artech House, Inc, Second Edition, 2005.
[7] E. Brookner, "Radar Technology" Artech House, 1991.
[8] A.Farina, Antenna-Based Signal Processing Techniques for Radar systems, Artech House, 1991.
[9] T.Hollis/R.Weir,The Theory of Digital Down Conversion Rev 1.2 26-06-2003
[10] CHESTON,T.C, AND FRANK,J.: array antennas chapter 11 in SKOLNIK, M.I(Ed):' Radar handbook' McGRAW HILL,1970.
[11] Charles H.Roth,'Digital Systems Design Using VHDL', PWS Publishing Company, First Edition, 1998.
[12] Douglas L Perry: VHDL programming by example, TATA McGRAW HILL, 4th edition, 2002.
[13] www.xilinx.com.

BIO DATA OF AUTHORS

Mr. DoddamaniGovindRaoborn on 2nd October 1978 at Gulbarga, Karnataka, India. He has completed his M.Tech in VLSI system Design in 2003 from NIT Warangal, Bachelor of Engineering in Electronics and Communication from Gulbarga University Gulbarga and secured 3rd rank to the University in the year 2000. He is working in LRDE, DRDO, Bangalore, India as Scientist and his areas of work include, FPGA based board design and Digital System Design.He has developed several control logics in VHDL, which has been used in the Radars. His expertise includes Digital system Design, Beam Steering and Digital Beam Forming for Active Phased array Radar.

Mr. AnantRaut received his B.E. degree in Electronics and Telecommunication in 2005, from SGSITS Indore, India. He worked as a lecturer in the Department of Electronics and Telecommunication of SVITS Indore. Presently he is working as a scientist in the Electronics and Radar Development Establishment (LRDE), Bangalore. His work contributions are in the area of Active Phased Array Radar digital subsystem design.

Mr. Renuka Prasad, born on 24th June1979 at Bangalore. He obtained his B.E. in Electronics and Communication Engineering from Bapuji Institute of Engineering And Technology, Kuvempu University, Davangere, Karnataka, India in the year 2002. He is working in LRDE, DRDO as Scientist since Oct 2002. He has designed and developed Digital Radar Systems using state of art technologies. He has significantly contributed in the development of phased array antenna systems. Presently he is working in the field of Multichannel digital receiver for the development of Active Phased Array Radar. He is also involved in the area of the digital beam forming algorithms design and digital beam steering logic design for an Active Phased array Radar. His areas of interest are digital system designs for Active Array Radars, Digital T/R modules and Digital Beam forming.

Mr. MdMustakim, received B.Tech Degree in Electronics and Communication Engineering from JamiaMilliaIslamia, University, New Delhi, in the year 2009.He is working in LRDE, DRDO as a Scientist since Feb 2010. His area of interest includes FPGA based Digital and RF System Design. Presently he is working in the development of Array Group receiver for the Active Phased Array Radar.

K Sreenivasulu received his Diploma in Electronics and Communication Engineering from S. V. Government Polytechnic, Tirupati, Andhra Pradesh, in the year 1987. He received his B.Tech Degree in Electronics and Communication Engineering from awaharlalNehruTechnologicalUniversity, Hyderabad, in the year 1995. He received his M.E degree in Micro Electronics Systems from Indian Institute Of Science, Bangalore, in the year 2004. He started his professional career as an Electronic Assistant in Civil Aviation Department where he worked from 1990 to 1995. At present he has been working in Electronics and Radar Development Establishment (LRDE), Bangalore, as a Scientist, since 1996.His area of work has been in Design, Development of RF and Microwave Subsystems, Digital Radar Systems, Beam Steering Controller for Active Aperture Array Radar. His interests include VLSI Systems and Programmable Controllers.